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Improved Reliability Memory's Module Structure for Critical Application Systems

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ABSTRACT
For critical application systems, which control nuclear power plants and other energy facilities, air, sea and ground vehicles, the needs to ensure their operability are increased. To fulfill this requirement, it is necessary to increase the technical readiness coefficient, the value of which increases with decreasing recovery time control system in case of fault of its constituent units. The main control system components critical applications are memory devices, which store programs and used for performing algorithms control. Semiconductor memory modules with automatic recovery functionality at multiple faults can be used in systems of critical applications protection and management where the use of fault-tolerant digital devices is a necessity due to the inability of traditional methods of repair by replacing the failed elements.
Keywords - Built-in, Memory, operability restoration, self-test

I. INTRODUCTION

Semiconductor memory modules with automatic recovery functionality at multiple faults can be used in systems of critical applications protection and management where the use of fault-tolerant digital devices is a necessity due to the inability of traditional methods of repair by replacing the failed elements.

At using the RAM for error checking, it is recommended to apply widespread utility Memtest86 +. However, when testing memory modules having this utility idle cycles during which memory components recovery may occur, however such a mode divergence may give inaccurate testing results. If testing found inefficient units, they should be replaced by serviceable. However, the time spent searching for the same memory module and to check the validity of the timing, as indicated in SPD. Significant time required to restore the system may lead to irreparable consequences for critical application systems.

Memory type ECC (Error Check & Correction / Error Correction Code), is able to automatically correct any single error and detect any dual. As long as the memory is functioning more or less normally, the opposition of entropy and a noise codes resolved in favor of the latter. However, the full or partial output of one or more memory modules fail, corrective ability of controlling codes are not enough and memory begins to work very unstable.

II. LITERATURE REVIEW

The known system with replacing rows and columns analyzing of internal memory for spares, which comprises a built-in self-test means (BIST), built-in recovery analysis (BIRA) performance means, switche the address codes, and data operations, the main memory cell array, spare rows and columns of cells, decoders of rows and columns of cells [1]. The disadvantage of this system is limited functionality due to a limited number of spare memory cells, which does not allow to carry out repairs at the component faults that cause inoperable whole discharge data. Also repair and restore an operability state of memory circuits during their operation is impossible.

The general approach of BIST for memory circuits includes the introduction of chip circuitry to generate additional tests, comparison and synchronization of responses with reference data. Typical structure of the memory chip with built-in self-test is shown in Fig. 1 and comprises a controller, addresses and data code generator, data comparator and switches, providing connection to the array of memory cells signals in the operation or test mode [2].

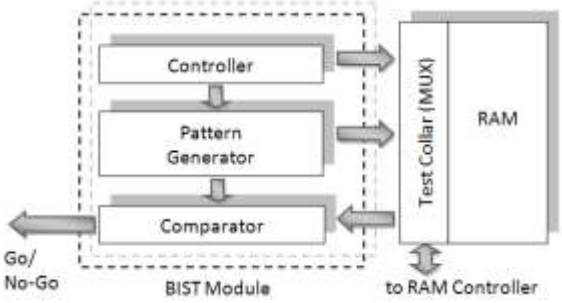

Fig. 1. Typical structure of a memory chip with built-in self-test

Using BIST architecture is cost-effective in the long term, by 2018, according to the SIA, 90% of silicon will be with integrated self-diagnostics, so that efforts must be focused on self-test embedded systems using programmable built-in resources.

When modifying BIST architecture is necessary to ensure rapid switching of the test process in the normal operation of the chip. Coverage of possible faults should increase with increasing period of operation chip, with hardware costs must be as low as possible, so as not to greatly increase the cost of implementing the new architecture [3-5].

III. METHODOLOGYE

In order to eliminate the disadvantages mentioned above, its proposed to include in the memory module an array of free data bits, which allows to record, store and retrieve data designed for storing in one or more data bits that are basically faulted the memory array. Upon detection of multiple faults the reconfiguration the structure of the memory module will be provided automatically instead of adding new hardware and software [6-17].

The implementation the embedded self-test significantly reduces the cost and increases the percentage of fault coverage, as it scans the operating frequencies and doesn't require an external test equipment, the cost of which is usually many times higher than the cost of the memory itself.

IV. RESULTS

ECC memory modules can detect and restore only the data bits, controlling bits are not subject to correction. Then, for example, for 64 data bits a single fault is allowed, and not for the 8 control bits. In this case, the probability of faults of the module with ECC is equal to the sum of the probabilities of faults of dual 64 data bits and the probability of faults of a single 8 controlling bits.

Graphs of the probability of faults of the memory module: q(t) – without using the proposed method; q1(t), q2(t), q3(t) и q4(t) – in carrying out 1, 2, 3 and 4 repairs are shown in Fig. 2. Also in red in Fig. 4 shows the probability of correct operation of the memory module without repair – p(t), in black the probability of double faults of 64 and single fault of 8 controlling bits of the memory module – q5(t).

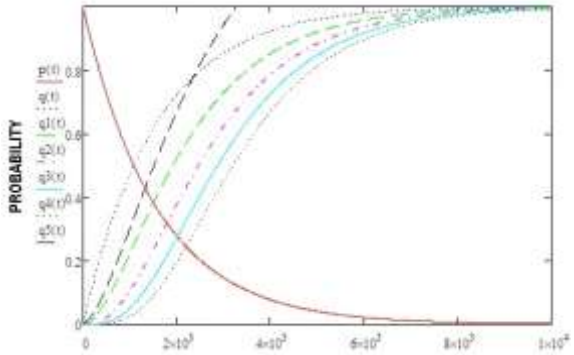

Fig. 2. Graphs of faults probability of the memory module

The histogram of the probability of faults of the memory module is presented in Fig. 3.

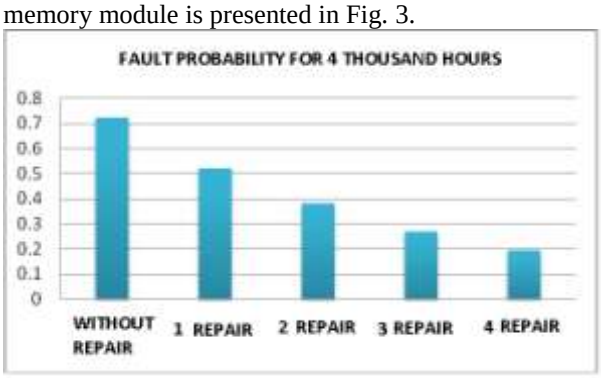

Fig. 3. Histogram of the probability of faults of the memory module

A block diagram of a memory module with efficiency automatic recovery under multiple faults is shown in Fig. 4.

The memory module includes a primary and backup storage arrays, the controller self-test and efficiency recovery, address code generators and data multiplexers of operation codes, address and data comparator, input and output data reconfigurator, efficiency recovery unit.

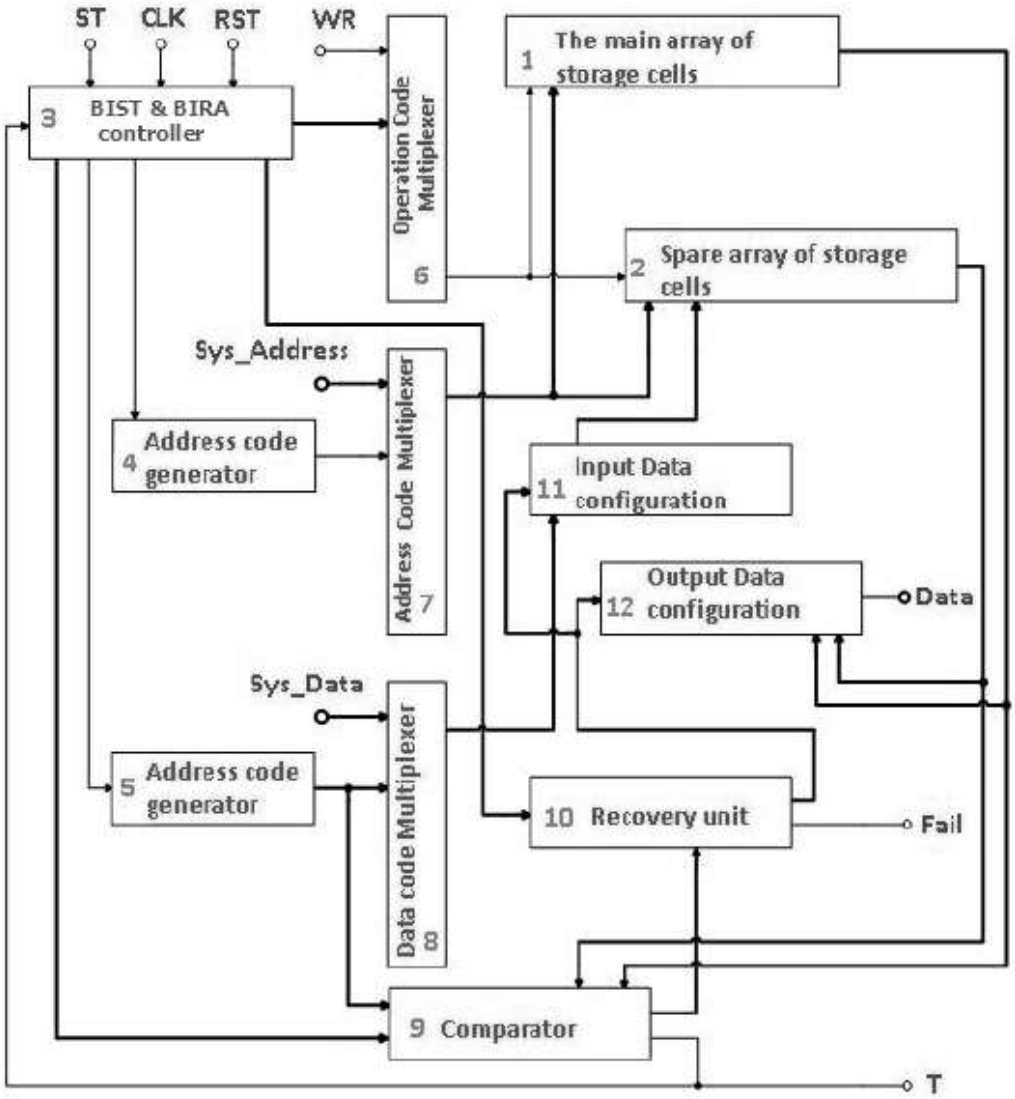

Fig. 4. Block diagram of a memory module with efficiency automatic recovery under multiple faults

From the Fig. 3 we can see that in carrying out four repairs, the probability of faults is reduced by 3.7 times compared with the module, where the repair is not performed. During the product's architecture designing, it's ensured to have highly diagnostic properties of the generated tests. This reduces the capacity of the test program by utilizing hardware and firmware method of tests forming that combines high performance with low hardware costs.

For example, the duration of memory chips test with a capacity of 640 Mbps and with a circulation time of 20 ns via the proposed product is 1.

In the product a multiprocessor structure of the device of diagnosing test of semiconductor memory products is used and a method of micro operations parallelization in tests algorithms.

The development of tests programs is carried out in the system of specialized interpreting programming language Prover, while ensuring the mobility of tests programs at change of parameters of the diagnosed products.

To reduce the cost of products are used the instrumental tools of development and debugging the programs of models verification of high-speed semiconductor memory chips, ensuring a clear and easy way of the modeling results presenting: a translator of the language Prover into VHDL language and a program of modeling results visualization.

V. CONCLUSION

Multiple increasing in the reliability of the control and information computer systems, which is especially important for critical applications systems, including the space equipments, aircraft equipments and other aerial devices .

Repair of storage control systems of unmanned aircraft will be possible in automatic mode without

the participation of the staff. This reduces the capacity of the programs test by utilizing hardware and firmware method of test forming that combines high performance with low hardware costs.

The weight of storage devices is reduced by duplicating not the whole product, but only a part of its constituent components.

Manufacturers of storage devices are proposed to purchase a manufacture license of memory modules with built-in tools that provide automatic efficiency recovery during multiple faults..

VI. Acknowledgements

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